IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:	Examiner: Ngan V. Ngo
Possley	Art Group: 2818
Application No.: 09/262,458	Confirmation No. 9423
Filed: 03/04/1999	
Patent No.: 6,974,978 B1	
Issued: 12/13/2005	
For: GATE ARRAY ARCHITECTURE	

Attn: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION

Dear Sir:

Upon review of the above-referenced Letters Patent, Applicant noted errors that are the mistake of both the Applicant and the Office. Those errors are as follows:

Fig. 3

Reference numeral 320 appears twice in the drawing. The second appearance of "320" should read –370--.

Insert reference numeral 300 so it applies to the entire flip-flop.

Column 8

Lines 12-15, "… first one or more interconnects interconnecting exclusively first size transistors to form a clock buffer of a logic component, consisting exclusively of first size transistors…" should read --… first one or more

interconnects interconnecting exclusively first size transistors of one or more adjacent ones of the plurality of arrangements of first size transistors to form a clock buffer of a logic component, consisting exclusively of first size transistors,…--.

Included with this submission is a Certificate of Correction, which includes a corrected Fig. 3, and it is respectfully requested that a Certificate of Correction be issued. This request for correction is made under the provisions of 37 CFR 1.322 and 1.323.

Payment by Deposit Account No. 500393 is included in the amount of $100.00 for the fee as set forth in 37 CFR § 1.20(a).

Respectfully submitted,

SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: 10/03/2007

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,974,978 B1

APPLICATION NO.: 09/262,458

ISSUE DATE : December 13, 2005

INVENTOR(S) : Possley

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Fig. 3
Reference numeral 320 appears twice in the drawing. The second appearance of "320" should read –370--. Insert reference numeral 300 so it applies to the entire flip-flop.

Column 8
Lines 12-15, "… first one or more interconnects interconnecting exclusively first size transistors to form a clock buffer of a logic component, consisting exclusively of first size transistors…" should read --… first one or more interconnects interconnecting exclusively first size transistors of one or more adjacent ones of the plurality of arrangements of first size transistors to form a clock buffer of a logic component, consisting exclusively of first size transistors,…--.

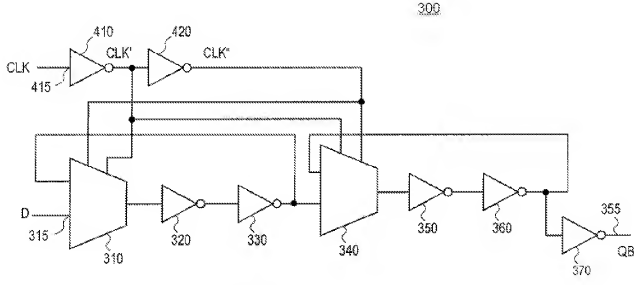

FIG. 3

MAILING ADDRESS OF SENDER (Please do not use customer number below):
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